GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
RAJYA SABHA
UNSTARRED QUESTION NO. 542
TO BE ANSWERED ON: 26.07.2024

ELECTRONIC CHIP DESIGN AND MANUFACTURING

542. SMT. SUMITRA BALMIK:

Will the Minister of ELECTRONICS & INFORMATION TECHNOLOGY be pleased to state:

(a) whether Government has narrowed down on any specific semiconductor chips whose indigenisation of design and manufacturing shall be prioritised based on their import dependencies, if so, the details thereof;
(b) whether Government is running any specific entrepreneurship development initiatives for startups looking to enter into the space, if so, the details thereof; and
(c) whether Government has done a study on the areas/sectors within the chip manufacturing ecosystem in which startups can venture into, if so, the details thereof?

ANSWER

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI JITIN PRASADA)

(a) to (c): The fabless semiconductor chip design area involves the design of IP (Intellectual Property) Cores, ASICs (Application Specific Integrated Circuit) and SoCs (System on Chips). This is driven by rapidly evolving requirements of semiconductor products in respect of power, performance, security etc. Government is focused on building the overall semiconductor ecosystem including semiconductor design and manufacturing. Government has approved the 'Semicon India Programme' with a total outlay of ₹ 76,000 crore for the development of semiconductor and display manufacturing ecosystem in the country. As part of this program, following schemes have been introduced:

i. The 'Design Linked Incentive (DLI) Scheme' offers support across various stages of development and deployment of semiconductor design for Integrated Circuits (ICs), Chipsets, System on Chips (SoCs), Systems & IP Cores and semiconductor linked design. The DLI scheme provides Chip design infrastructure support; as well as financial incentives for 'Product Design Linked Incentive' of up to 50% of the eligible expenditure subject to a ceiling of ₹15 Crore per application and 'Deployment Linked Incentive' of 6% to 4% of net sales turnover over 5 years subject to a ceiling of ₹30 Crore per application. Under the DLI Scheme, twenty-eight (28) domestic Start-ups/ MSMEs companies have received support and are in the process of designing IP Cores, ASICs & SOCs for applications not limited to the following - Automotive, Mobility, Compute, Communication etc.
ii. 'Modified Scheme for setting up of Semiconductor Fabs in India' supports the Companies / Consortia / Joint Ventures proposing to set up a Silicon CMOS based Semiconductor Fab in India for manufacturing Logic / Memory / Digital ICs / Analog ICs / Mixed Signal ICs / SoCs.
iii. Modified Scheme for setting up of Display Fabs in India.

iv. Modified Scheme for setting up of Compound Semiconductors / Silicon Photonics / Sensors Fab / Discrete Semiconductors Fab and Semiconductor Assembly, Testing, Marking and Packaging (ATMP) / OSAT facilities in India**.**

v. In addition to the above schemes, Government has also approved modernisation of the existing semiconductor manufacturing facility - Semi-Conductor Laboratory (SCL), Mohali as a brownfield Fab.

Under the Chips to Startup (C2S) Programme being implemented at 113 academic institutions/ R&D organizations/ Start-ups/ MSMEs, 85,000 number of high-quality and qualified engineers are being trained in several areas. These include Very large-scale integration (VLSI) and Embedded System Design as well as development of 175 ASICs (Application Specific Integrated Circuits), working prototypes of 20 System on Chips (SoC), 30 FPGA based designs and 30 IP Cores over a period of 5 years.

Based on the requirement of user organizations, MeitY from time-to-time invites proposals for design, development & deployment of Chipsets which domestic Start-ups/ MSMEs can participate. Some of these chipsets include, but are not limited to, the following:

(i) Design, development and deployment of integrated chipset of NavIC (Navigation with Indian Constellation) Receivers in the country;
(ii) Design, development and deployment of secure Systems on Chips (SoCs) using Indian owned processor based on open-source ISA;
(iii) Design and development of series of microprocessors based on open-source ISA (Instruction Set Architecture).

As per the inputs received from the Department of Telecom (DoT), Task Force was constituted by DoT on High volume Telecom Chipset Development; which, inter-alia, recommended development of six chipsets for specific use of telecom equipment as per following details:

Three types of chips for Consumer Premise Equipment (CPEs)

(i) Next-generation Broadband CPE chipset
(ii) 5G Modem + Radio chip for Dongles/ loTs (Internet of Things)/ Mobile Edge/ Satcom
(iii) Multi-radio chip Microcontroller for Gateways

Three types of chips for Network Infrastructure Equipment

(i) xPON (Passive Optical Network) OLT (Optical Iine Terminals) chips for fiber broadband infra equipment
(ii) Digital Signal Processor for Radio and Baseband Processing
(iii) L2/ L3 Packet Switch chipsets with Embedded Processor

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