GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
RAJYA SABHA
UNSTARRED QUESTION NO. 1341
TO BE ANSWERED ON: 06.12.2024

UTILISATION OF FUNDS UNDER PDSDME FOR SEMICONDUCTOR UNITS

1341. SMT. RENUKA CHOWDHURY:

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGY be pleased to state:

(a) the funds utilised for semiconductor units under the Programme for Development of Semiconductors and Display Manufacturing Ecosystem (PDSDME) since its inception, year-wise, project-wise;
(b) whether Government has received proposals for establishment of semiconductor units and assembly plants under the said scheme and the Modified Programme for Semiconductors and Display Fab Ecosystem (MPSDFE), if so, the details of the proposals received; and
(c) whether it is a fact that the recently approved semiconductor unit by Kaynes Semicon Pvt Ltd, in Sanand, Gujarat, was initially planned to be established in Telangana, if so, the reasons for relocating the plant from Telangana to Gujarat?

ANSWER

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI JITIN PRASADA)

(a) and (b): Government approved Programme for Development of Semiconductors and Display Manufacturing Ecosystem in India ("Semicon India Programme") on 15.12.2021 with a total outlay of INR 76,000 crore. The Programme was subsequently modified by the Cabinet, which provides:

i. Fiscal support of 50% of the project cost on *pari-passu* basis for setting up of Silicon Complementary Metal-Oxide-Semiconductor (CMOS) based Semiconductor Fabs in India.

ii. Fiscal support of 50% of Project Cost on *pari-passu* basis for setting up of Display Fabs in India.

iii. Fiscal support of 50% of the Capital Expenditure on *pari-passu* basis for setting up of Compound Semiconductors / Silicon Photonics (SiPh) / Sensors (including Micro-Electro-Mechanical Systems) Fab/ Discrete Semiconductor Fab and Semiconductor Assembly, Testing, Marking and Packaging (ATMP) / Outsourced Semiconductor Assembly and Test (OSAT) facilities in India.

iv. Product Design Linked Incentive of up to 50% of the eligible expenditure subject to a ceiling of ₹15 Crore per application and also "Deployment Linked Incentive" of 6% to 4% of net sales turnover over 5 years subject to a ceiling of ₹30 Crore per application for incentivising chip design.

Government has also approved modernisation of Semi-Conductor Laboratory, Mohali to enhance efficiency and cycle time.

Under Semicon India Programme, Government has approved five (5) semiconductor projects with cumulative investment of around Rs. 1 lakh 52 thousand crore. Further, 15 semiconductor design companies have also been approved under the Design Linked Incentive Scheme to design chips for Indian products. Additionally, 41 semiconductor design companies have been approved for access of the tools required for designing the chips (called EDA tools) which is being made available by National EDA Tool Grid setup at ChipIN Centre at C-DAC Bengaluru.

(c): Kaynes Semicon Pvt. Ltd had decided to setup the semiconductor facility at Sanand Gujarat. The decision regarding the location of Semiconductor manufacturing facility lies with companies proposing to setup such facilities based on various parameters, including availability of stable power supply, sufficient water supply and State Government incentives.

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